WHAT IS CLAIMED IS:

1. An integrated circuit for modem including:

a hardware unit for conducting an error correction processing, interleave processing and digital signal processing for transmission and reception data;

an instruction RAM comprising a plurality of banks, which functions as a cache memory of an external instruction RAM; and

a CPU which executes an instruction which is prefetched to the instruction RAM for controlling said hardware unit, wherein that said CPU and said hardware time-divisionally share part of the banks of said instruction RAM.

2. An integrated circuit for modem as defined in Claim 1 in which said hardware unit divides the banks of said instruction RAM and uses part of the banks of said instruction RAM as a memory for interleave processing.

3. An integrated circuit as defined in Claim 1 in which said circuit comprises an RAM controller which conducts controlling so that instructions are prefetched from said external instruction ROM to said instruction RAM on a bank basis to cause said instruction RAM to function as a cache memory of said external instruction ROM and conducts controlling to cause said CPU and said hardware unit to time-divisionally share part of the banks of said instruction RAM.

4. An integrated circuit as defined in Claim 3 in which said circuit comprises an RAM controller which conducts controlling so that instructions are prefetched from said external instruction ROM to said

instruction RAM on a bank basis to cause said instruction RAM to function as a cache memory of said external instruction ROM and conducts controlling to cause said CPU and said hardware unit to time-divisionally share part of the banks of said instruction RAM.

5. An integrated circuit for modem as defined in Claim 3 in which said RAM controller receives data, address and write control signal from an interleave RAM interface of said hardware unit and outputs them to part of the banks of said instruction RAM and outputs them to an interleave RAM interface of said hardware unit by selecting the data output of part of the banks of said hardware unit during the transmission and reception of the data.

6. An integrated circuit for modem as defined in Claim 4 in, which said RAM, controller comprises

a higher order address to which high order addresses are input from an interleave RAM interface of said hardware unit and are decoded and from which a bank selection signal for the interleave RAM is output;

a gate circuit to which a write control signal is input from the interleave RAM interface of said hardware unit and which is controlled by said bank selection signal for outputting a bank write control signal for the interleave RAM therefrom;

a (first) multiplexer to which data is input from the interleave RAM interface of said hardware unit and which switches to part of the banks of said instruction RAM in response to a connection switching signal for outputting data thereto;

a (second) multiplexer to which an address and said bank write

control signal are input from the interleave RAM interface of said hardware unit and said gate circuit and switches to part of the banks of said instruction RAM in response to said connection switching signal for outputting them thereto; and

a selector which selects a data output from the part of the banks of said instruction RAM in response to said bank selection signal and to output the data to the interleave RAM interface of said hardware unit.

7. An integrated circuit for modem as defined in Claim 6 in which said RAM controller comprises a control register in which commands which are preset by said CPU are stored and in which said connection switching signal is generated corresponding to the content of control register.